We claim:

1. A method of fabricating a sub-micron MOS transistor comprising:

preparing a substrate, including isolating an active region therein;

depositing a gate oxide layer;

depositing a first selective etchable layer over the gate oxide layer;

depositing a second selective etchable layer over the first selective etchable layer;

etching the structure to undercut the first selective etchable layer;

implanting ions in the active region to form a source region and a drain region;

removing the remaining first selective etchable layer and the second selective etchable layer;

depositing a gate electrode; and

depositing oxide and metallizing the structure.

2. The method of claim 1 wherein said depositing a first selective etchable layer includes depositing a layer of silicon nitride, and wherein said depositing a second selective etchable layer includes depositing a layer of silicon oxide.

3. The method of claim 1 wherein said depositing a first selective etchable layer includes depositing a layer of polysilicon, and wherein said depositing a second selective etchable layer includes depositing a layer of silicon nitride.

4. The method of claim 1 wherein said depositing a first selective etchable layer includes depositing a layer of polysilicon, and wherein said depositing a second selective etchable layer includes depositing a layer of silicon oxide.

5. The method of claim 1 wherein said depositing a gate electrode includes depositing a layer of material taken from the group of materials consisting of doped polysilicon and metal.

6. The method of claim 1 wherein said implanting includes implanting Arsenic ions at a dose of between about $1 \cdot 10^{15}$ cm^{-2} to $5 \cdot 10^{15}$ cm^{-2}, and an energy level of between about 30 keV to 70 keV.

7. The method of claim 6 wherein said implanting includes forming a LDD source region and an LDD drain region adjacent the gate region.

8. The method of claim 7 wherein said implanting includes implanting ions to provide an ion concentration in the source region and in the drain region of between about $1 \cdot 10^{20}$ cm^{-3} to $1 \cdot 10^{21}$ cm^{-3}, and wherein the ion concentration the LDD source region and in the LDD drain region is between about $5 \cdot 10^{18}$ cm^{-3} to $5 \cdot 10^{18}$ cm^{-3}.

9. A method of fabricating a sub-micron MOS transistor comprising:

preparing a substrate, including isolating an active region therein;

depositing a gate oxide layer;

depositing a first selective etchable layer over the gate oxide layer;

depositing a second selective etchable layer over the first selective etchable layer;

etching the structure to undercut the first selective etchable layer;

implanting ions in the active region to form a source region and a drain region, including forming a LDD source region and an LDD drain region adjacent the gate region;

removing the remaining first selective etchable layer and the second selective etchable layer;

depositing a gate electrode; and

depositing oxide and metallizing the structure.

10. The method of claim 9 wherein said depositing a first selective etchable layer includes depositing a layer of silicon nitride to a thickness of between about 200 nm to 500 nm, and wherein said depositing a second selective etchable layer includes depositing a layer of silicon oxide to a thickness of between about 20 nm to 100 nm.

11. The method of claim 9 wherein said depositing a first selective etchable layer includes depositing a layer of polysilicon, and wherein said depositing a second selective etchable layer includes depositing a layer of silicon nitride, wherein the thickness of both layers is between about 200 nm and 500 nm.

12. The method of claim 9 wherein said depositing a first selective etchable layer includes depositing a layer of polysilicon to a thickness of between about 200 nm to 500 nm, and wherein said depositing a second selective etchable layer includes depositing a layer of silicon oxide to a thickness of between about 20 nm to 100 nm.

13. The method of claim 9 wherein said depositing a gate electrode includes depositing a layer of material taken from the group of materials consisting of doped polysilicon and metal.

14. The method of claim 9 wherein said implanting includes implanting Arsenic ions at a dose of between about $1 \cdot 10^{15}$ cm^{-2} to $5 \cdot 10^{15}$ cm^{-2}, and an energy level of between about 30 keV to 70 keV.

15. The method of claim 9 wherein said implanting includes implanting ions to provide an ion concentration in the source region and in the drain region of between about $1 \cdot 10^{20}$ cm^{-3} to $1 \cdot 10^{21}$ cm^{-3}, and wherein the ion concentration the LDD source region and in the LDD drain region is between about $5 \cdot 10^{18}$ cm^{-3} to $5 \cdot 10^{19}$ cm^{-3}.

16. A sub-micron MOS transistor comprising:

a substrate; and

an active region, including a gate region having a length of less than one micron; a source region including a LDD source region; and a drain region including a LDD drain region; wherein the ion concentration in said source region and in said drain region is between about $1 \cdot 10^{20}$ cm^{-3} to $1 \cdot 10^{21}$ cm^{-3}, and wherein the ion concentration in said LDD source region and in said LDD drain region is between about $5 \cdot 10^{18}$ cm^{-3} to $5 \cdot 10^{19}$ cm^{-3}.

17. The MOS transistor of claim 16 which further includes an insulating oxide layer thereover and a source electrode, a gate electrode and a drain electrode.